Multi-Walled Microchannels: Free-Standing Porous Silicon Membranes for Use in μTAS

R. Willem Tjerkstra, Johannes G. E. Gardeniers, John J. Kelly, and Albert van den Berg

Abstract—**Electrochemically formed porous silicon (PS) can be released from the bulk silicon substrate by underetching at increased current density. Using this technique, two types of channels containing free-standing layers of PS were constructed, which were called multi-walled microchannels (MW μCs). They can be used in devices like microsieves, microbatteries, and porous electrodes. Two types of MWμC were made: the "conventional" version, consisting of two or more coaxially constructed microchannels separated by a suspended PS membrane, and the buried variety, where a PS membrane is suspended halfway an etched cavity surrounded by silicon nitride walls. The latter is more robust. The pore size of the PS was measured using transmission electron microscopy and field emission gun scanning electron microscopy (FEGSEM) and found to be of the order of 7 nm. [462]**

Index Terms—**Electrochemical etching, microsieve, pore size, porous silicon, silicon micromachining.**

I. Introduction

IN MICROMECHANICS, porous silicon (PS) has been used for a number of purposes. It is frequently utilized as a sacrificial material because it can be formed by highly selective electrochemical processes and can be etched away using relatively harmless solutions like photoresist developer [1]–[4]. The large surface area of PS and its relative inertness make it an ideal material to increase the area of an analytical device [5]. Oxidized PS has also been used as an insulating material in gas sensors [6], whereas metallized PS can be used in microelectronics [7].

PS layers can be released from the bulk substrate by increasing the current density during the electrochemical formation. This phenomenon has been used by Kanemitsu to study the optical properties of PS layers [8]. If the PS can be fixed locally to a rigid support, many new applications become possible. In this paper, the formation of such structures, which we call multi-walled microchannels (MWμCs), is described. These are channels containing one or more free-hanging layers of PS attached to some material. The structures can be used as for instance porous electrodes or as sieves, but many other applications are feasible. Unlike materials such as aluminum oxide or zeolites, these structures can be directly incorporated in a micro total analysis system (μTAS) design at precisely the right place and with adjustable pore sizes, in a one-run process. This makes the MWμCs very promising for μTAS applications.

In this paper, the formation of MWμCs is described. Two designs were made: a simple channel containing a porous layer suspended by the mask material, and a buried PS layer. The latter design is more robust and therefore has more potential in a device. Attempts were made to measure the pore sizes of the PS layers.

II. PS Formation and Properties

Since its discovery by Uhlir [9] in 1956, PS has been the subject of intense research. Its chemical composition and structure have been thoroughly studied [10]–[14]. More recently, the discovery of strong visible luminescence from PS at room temperature by Canham [15] in 1990 initiated many investigations into the optical properties of this material [8], [16], [17]. The mechanical properties of PS have also been thoroughly studied [3], [18]–[20].

PS can be made by anodically etching p-type silicon in fluoride containing solutions using a current density lower than that of the first peak in the current-potential curve [21]. The height and place of the first current peak depends on the fluoride concentration, the hydrodynamics of the system, and the resistivity of the wafers. The current density during formation of PS can be up to 100 mA/cm^2, depending on the desired pore size and the fluoride concentration. At potentials higher than the peak, potential electropolishing will occur. The pore size and porosity can be measured using, for instance, TEM pictures [13] and adsorption isotherms [22], [23]. The pore sizes reported in refs. [22] and [23] vary between 2–11 nm, depending on the hydrogen flouride (HF) concentration and the current density: the higher the HF concentration and the lower the current density, the smaller the pore size and the porosity will be. The porosity of PS formed from heavily doped p-Si at 10% HF and 10 mA/cm^2 is around 70% [23]. The porosity of PS formed from lightly doped silicon under the same conditions is much higher. According to Smith *et al.* [24], the rate of formation of PS depends on the hole flux from the bulk to the substrate surface.

The doping density of the substrate has a significant effect on the 3-D structure of the PS [13]. PS etched in heavily doped substrates exhibits a structure with long, branched pores. This PS has a reasonably large mechanical strength. In lightly doped substrates, the PS formed looks like a conglomeration of very tiny bubbles. The mechanical strength is considerably lower [23]. Free-standing PS can be made by first etching in the PS range, and subsequently increasing the current density to the electropolishing range [8], [24]. Fig. 1 shows how a MWμC can be made. A channel is etched under a mask using a high

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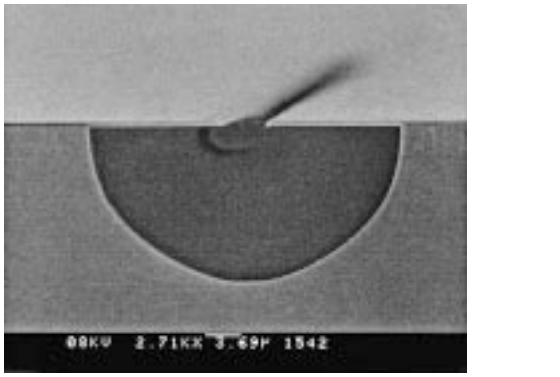
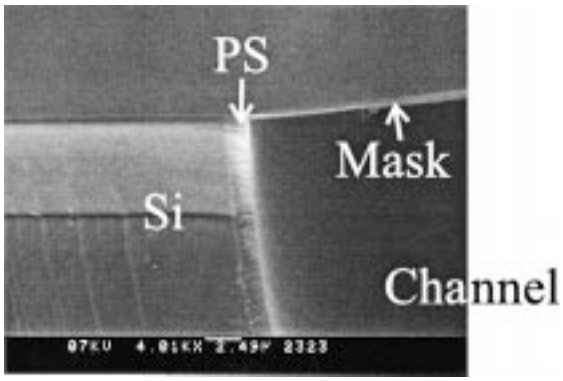
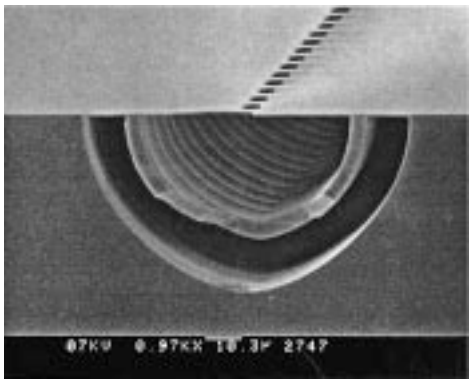


(a)



(b)



(c)

Fig. 1. Process scheme for creating the MWμCs. (a) Etch channel. (b) Form PS. (c) Underetch PS.

current density Fig. 1(a). In the polishing range, the etching is mass-transport controlled and therefore isotropic. This results in rounded profiles, as shown. After a certain time, the current density is lowered and a porous layer is formed Fig. 1(b). Subsequently, the current density is increased and the porous layer is underetched Fig. 1(c). Because it is still connected to the mask material, it is now a part of an MWμC. The dimensions of the channels can be controlled by the etch time and the mask opening. Instead of first etching a channel, it is also possible to first etch the PS and afterwards underetch it at a high current density. A channel covered with a flat layer of PS is then formed. Another possibility is etching the channel anisotropically using KOH or RIE-etching to get different shapes. After defining the shape of the PS, a MWμC can be etched using the method described. It is possible to subsequently close the mask opening by growing a layer of, for instance, silicon nitride that is thick enough to fill the mask opening. Of course, the pores of the PS will also be closed in this way. Instead of closing the mask, one can also choose to modify the PS by for example coating it with a metal layer [7] or nitridation [25].

III. Experiments and Results

A. Fabrication of MWμCs

1) Conventional Version: We made MWμCs by etching channels in a p-type silicon wafer, using LPCVD silicon-rich silicon nitride as a mask material. The wafers used were p-type {100} boron-doped, with a resistivity of 0.01–0.018 Ωcm (Wacker). They were covered with 500-nm LPCVD silicon-rich silicon nitride. Before deposition of the silicon nitride layer, the wafers were dipped in 1% HF (from 50% HF, Merck VLSI selectipur, diluted with DI water) to remove the native oxide layer. The silicon nitride on the backside of the wafers was removed using an RIE process, and a layer of 750-nm aluminum was evaporated and annealed for 30 min in a water-vapor rich atmosphere at 450 °C. The silicon nitride on the front side of the wafer was patterned using photolitography and RIE. The samples were etched in an aqueous 5% HF solution, using an EG&G 366-A potentiostat as a current source and an Orion 900 600 Ag/AgCl double-junction HF-resistant reference electrode, using the process shown in Fig. 1.

First, a channel was etched at a potential of 3 V versus Ag/AgCl (current density 180 mA/cm^2) for about 10 min. The rate of formation of the channel is in the order of 1 μm/min. Because the etching for these channels is isotropic, the etch rate not only depends on the HF concentration and the current density, but also on the local structure density [26]. After etching the channel, the potential was switched to 0 V versus Ag/AgCl and the sample was etched for 15 min (current density 40 mA/cm^2). A layer of PS was formed on the channel wall, with a rate of around 0.3 μm/min. We found that under the conditions we used the maximum thickness of the PS was around 10 μm. After this thickness was reached, the PS began to crack and peel off the surface, presumably due to internal stress. In the final step, the PS was etched free by switching the potential back to 3 V and etching for another 15 min. The etch rate of the silicon beneath the PS wall depends mainly on the rate of diffusion of the reactants through this wall, and can be quite low (around 0.1 μm/min). After etching, the samples were rinsed with deionized water and dried on air.

The PS made this way has small pores. The direction of the pores was found to be independent of the crystal lattice. This is in disagreement with the results of other researchers, who found a dependence of the pore direction on the crystal lattice [17], [24], [27].

In Fig. 2, a MWμC created with the method described above is shown. By repeatedly switching the potential to high and low values, multiple free-standing walls were made. It is also possible to make a flat porous layer by first etching at a low current density region, and subsequently increasing the current density to produce the channel. The main problem in making devices using the technique described above is the reproducibility of

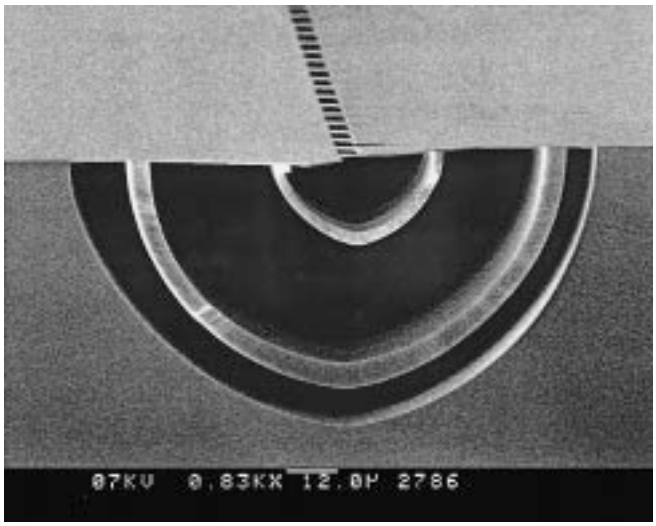


Fig. 2. SEM photograph of a MWμC containing two porous layers.

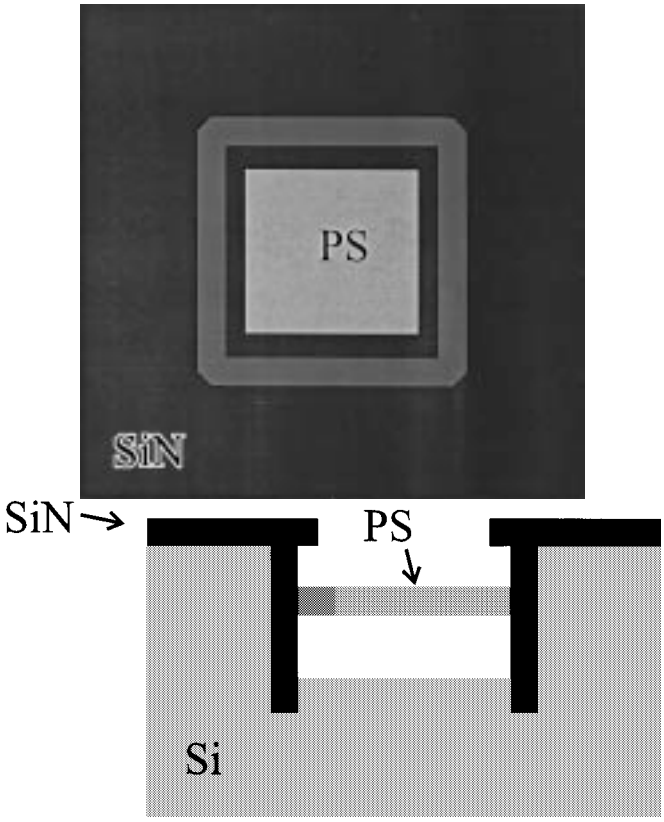


Fig. 3. Schematic view of a buried PS layer.

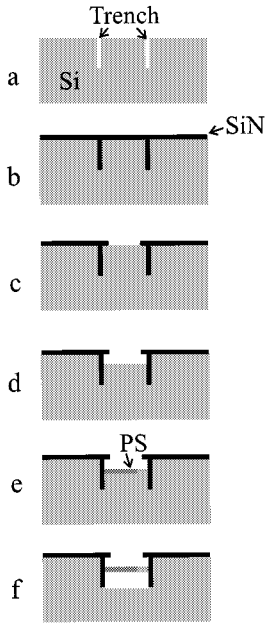


Fig. 4. Process scheme for fabrication of the buried PS layers.

the attachment of the PS to the mask material. The porous Si can tear off because of the presence of a thin layer of native oxide between the mask and the silicon wafer that will be etched away in the HF solution. Another cause of detachment can be the fact that the PS has a larger lattice constant than bulk silicon [28], leading to stress in the PS/mask interface. The larger lattice constant can be caused by oxidation of the PS surface. The breaking of the PS can also be caused by stress due to capillary effects during the drying of the sample. A fourth cause may be the bending of the mask material due to intrinsic stress. This can be diminished by defining the channels by a row of holes rather than a slit in the mask material. In Fig. 1(b), a channel made using a slit in the mask material is shown. The mask material is bent upwards. Using a row of holes instead of a slit prevents this (Fig. 2). Another possible solution for this problem is the use of a different LPCVD process. At the moment, we do not know which of the above-mentioned phenomena is the most important cause for breaking. In an attempt to solve the problems described above, a totally new design was made which increases the strength of the structure considerably. In the next sections, this design will be described.

2) Buried PS Layers: In a usable design of an MWμC, it must be possible to make stable connections to the structure. In our view, the key to the solution of this problem is that the flexibility of the support of the PS to the substrate must be minimized to prevent the PS from breaking.

A design that has these characteristics is shown in Fig. 3. It consists of a silicon nitride "pipe" in which the PS is formed. This structure has several advantages over the previously described structures. The silicon nitride walls are fixed to the bulk silicon so they cannot move. Because the PS is attached to a rigid surface, it is much less vulnerable and connections can easily be made by, for instance, gluing a connector on the wafer surface. The structures were made following the scheme in Fig. 4. First, a trench was etched in the wafer using the techniques for the fabrication of buried channels, as described in [26], [29], [30] Fig. 4(a). The trench was square-shaped, 50×50 μm, had a width of 4 μm and a depth of 40–50 μm. It was filled by growing LPCVD silicon-rich silicon nitride Fig. 4(b). The silicon nitride inside the area surrounded by the trench was subsequently etched away Fig. 4(c). The silicon nitride at the back of the wafer was also removed and 750 nm of aluminum was evaporated. The Al was annealed for 30 min in a water-vapor-rich atmosphere at 450 °C. The wafers were etched in 5% HF at alternatingly high (3 V versus Ag/AgCl) and low (0 V versus Ag/AgCl) potential Fig. 4(d)–(f). The result is shown in Fig. 5. In this figure, a cross section of a silicon nitride pipe containing one layer PS is

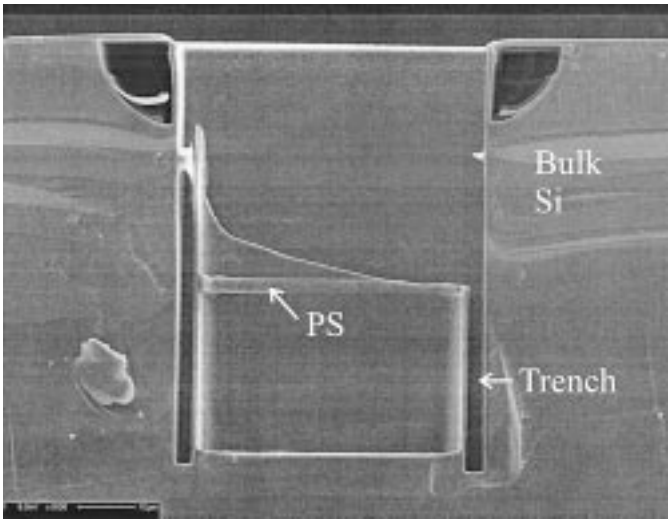


Fig. 5. Cross section of a buried PS layer.

shown. The buried layer is created by first etching at 3 V versus Ag/AgCl for 10 min, then at 0 V for another 10 min, and subsequently etching at 3 V for 10 min. Unfortunately, most of the PS was lost during the breaking of the wafer.

For the experiment of Fig. 5, the trench was not completely filled with silicon nitride, because this takes a long time. Therefore, when etching the silicon nitride in the area surrounded by the trench, the silicon nitride in the corner is etched open, and during electrochemical etching, holes appear at the wafer surface [30]. This will not happen when the trench is completely filled. As in the conventional version, multiple layers can also be etched.

B. Measurement of Pore Sizes

The pore sizes of the PS proved to be very difficult to measure. The most common techniques to determine pore size are transmission eectron microscope (TEM) [13] or adsorption isotherm [22], [23] measurements. Other methods include mercury porosimetry [31], [32] and the use of (field emission gun) scanning electron microscope (FEG)SEM pictures. For measuring adsorption isotherms, much material is needed (in the order of grams), and since we only have very small amounts of PS, this technique is not usable for the MWμCs. The same holds for the mercury porosimetry. Because for TEM a very tiny sample is enough to do reliable measurements, and the resolution of the FEGSEM is high enough to reveal the pores (as opposed to a normal SEM), we used TEM and FEGSEM techniques.

1) TEM: In a TEM, electrons are passed through the sample and detected on a fluorescent plate. The light parts of the image show a high electron flux through the sample, whereas the dark parts show a low electron flux. For TEM measurements, very thin samples transparent for the electrons are needed. For making these samples, we used a focused ion beam (FIB) etcher (FEI 2000), normally used to modify integrated circuits on chips. The specimens were made as follows: a channel coated with a layer of PS was made by first etching for 15 min at 3 V versus Ag/AgCl and afterwards for 5 min at 0.0, 0.1, or 0.2 V versus Ag/AgCl. The wafers used were the same as those used for making the MWμCs. After etching the channel

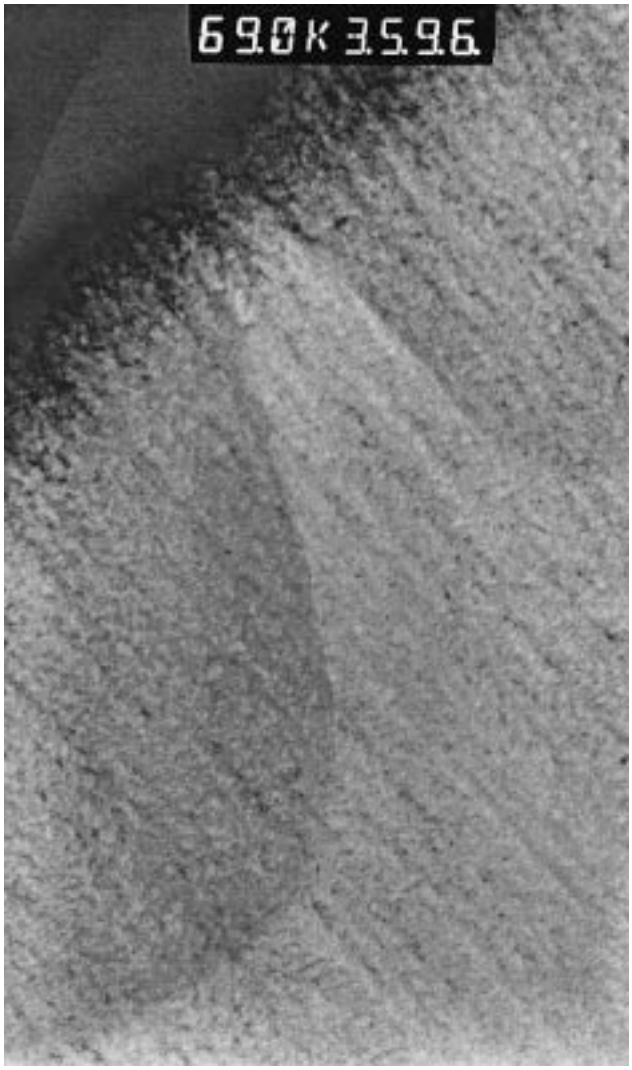


Fig. 6. TEM picture of PS.

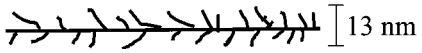


Fig. 7. Schematic drawing showing a branched pore. The diameter of the pores measured using TEM may be the space taken up by a pore and its branches.

the wafer was cut perpendicular to the channel into pieces of approximately 30–40 -μm wide. These were glued to a copper horseshoe-shaped TEM grid and mounted in the FIB. In the FIB, most of the PS was removed, leaving a very thin tapered wall of approximately 47-nm thickness at the top (estimated from EELS measurements) and 200 nm at the bottom, standing in the middle of the channel. The lowest thickness, although thin enough to make pictures, was still too thick to be able to measure pore sizes reliably. Because etching with a FIB is a physical process, the pore size of the PS is not affected.

In Fig. 6, a TEM picture of PS is shown. From this picture, we estimated an average pore size of 13.4 $\pm$4 nm by measuring the width of 10 light areas which we assume to be pores. It is, however, impossible to decide whether the dark colored areas are really the pores or consist of pores and short branches, as indicated in Fig. 7, so the value determined in this way only gives an upper limit of the pore size.

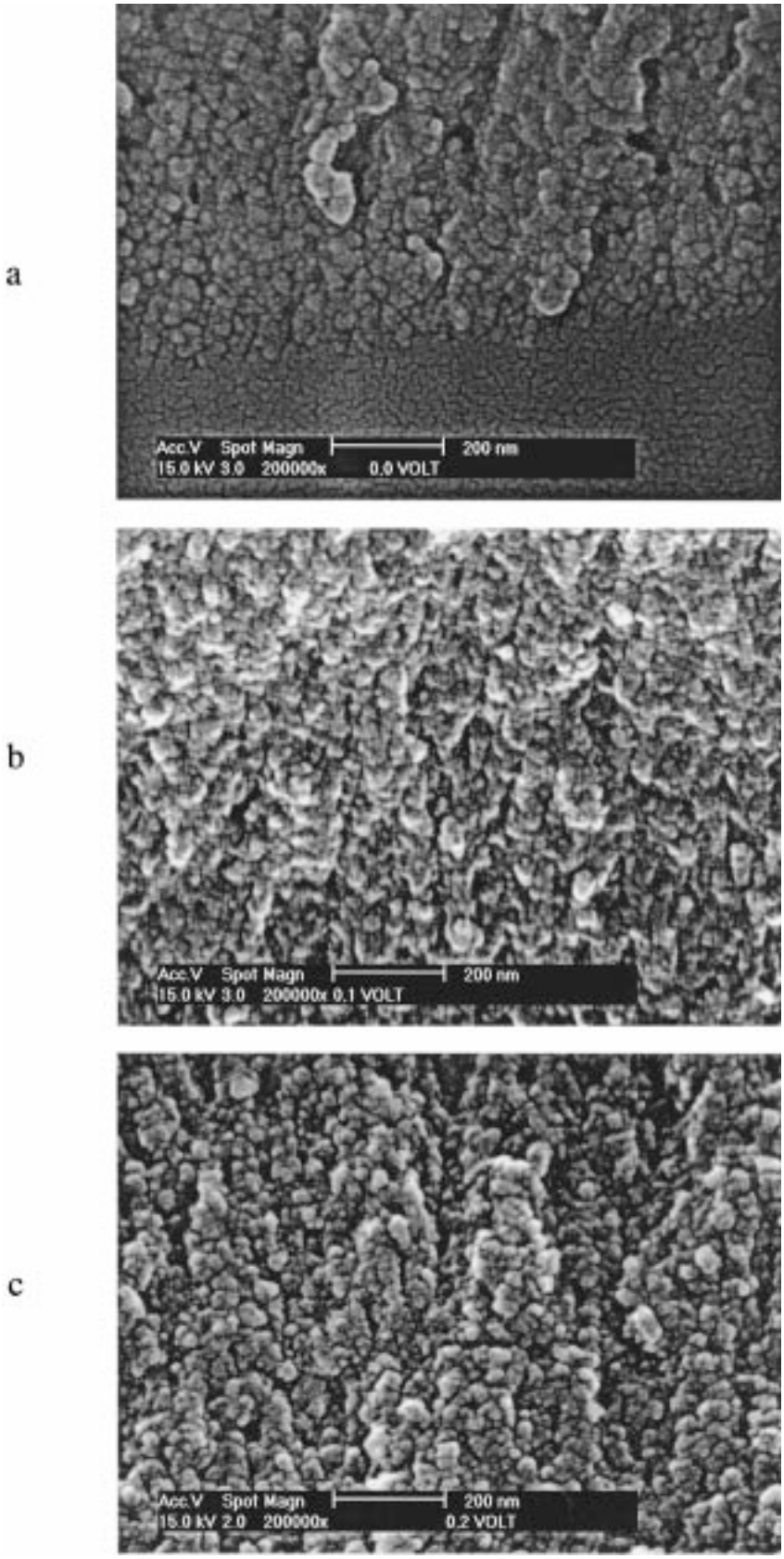


Fig. 8. FEGSEM pictures of PS etched in 5% HF at potentials of: (a) 0.0 V; (b) 0.1 V; and (c) 0.2 V versus Ag/AgCl.

2) FEGSEM: In a FEGSEM, the imaging electrons are generated from a sharp tip instead of being emitted from a glowing coil. Because the temperature of the tip is much lower, the velocity distribution of the electrons is narrower. The electron beam is also finer because of the small size of the electron source [33]. The fine electron beam allows the use of a lower accelerating

TABLE I
PORE DIAMETERS AS A FUNCTION OF APPLIED POTENTIAL

Applied potential (V vs Ag/AgCl)	mean pore diameter (nm)	σ_{n-1} (nm)
0	6.6	0.95
0.1	7.5	0.92
0.2	7.2	1.5

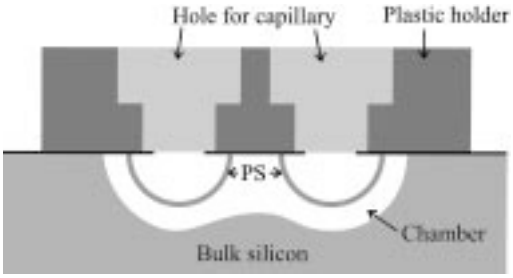


Fig. 9. A sieve can be made by etching through two closely separated holes and gluing a connector to the resulting structure.

voltage, which results in less penetration in the sample. Therefore, the FEGSEM can achieve a much higher resolution than a conventional SEM (0.8–1.2 nm; maximum obtainable resolution with SEM is 3–4 nm).

FEGSEM pictures were taken of PS samples etched in 5% HF using potentials of 0.0, 0.1, and 0.2 V versus Ag/AgCl. Examples are shown in Fig. 8. Using a marking gauge, we measured the diameter of ten pores from FEGSEM pictures of samples etched at the different potentials. The results are shown in Table I. This table clearly shows that the pore diameter is only slightly influenced by the current density in this region. This was also found by Smith *et al*. [34], [21]. The fact that pore sizes of the order of 7 nm were measured supports the suspicion that the pore sizes measured from the TEM sample correspond to the widths of the pores plus the branches, as shown in Fig. 7.

IV. POTENTIAL APPLICATION OF MWμCs

MWμCs can be used in a number of applications. A device that directly comes to mind is a sieve for the separation of very small particles. It can be made using the "conventional" technique by etching through two closely placed holes (Fig. 9). First two unconnected cusps that are not connected to each other are etched at a high current density. After that, the current density is lowered and PS is formed. The pore size can be controlled by the current density. Subsequently, the current density is increased and a cavity connecting the two PS sieves is formed. After etching, the sieve structure the pore size of the PS can be decreased by growing a layer of for instance silicon nitride on the PS surface [25], or oxidizing the PS. If necessary, the pore size can be increased by chemical etching in HF solution with or without an oxidizing agent [35], [36].

The surface properties of the PS can also be altered by attaching silanes with certain end groups. For instance, a silane with a -CF_3 end group will decrease the surface energy of the

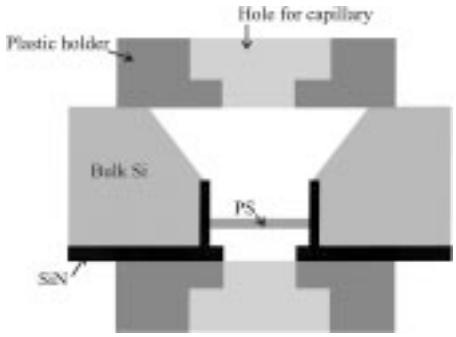


Fig. 10. Sieve made from a buried PS structure.

PS. Finally a plastic holder for two capillaries can be glued to the structure.

The structure shown in Fig. 9 will be very fragile and difficult to make and handle. A better sieve can be made using the buried technique. Part of the wafer is removed by etching in a KOH solution, to yield eventually the structure shown in Fig. 10. Work is currently in progress to investigate the feasibility of this design. A sieve also offers a new way to measure the pore size: by forcing particles with known diameters through the sieve the pore sizes can be determined.

V. CONCLUSION

Two types of MW μCs have been constructed in a one-run multistep process by etching p-type silicon anodically in an HF solution and switching the potential back and forth from a high to a low value. The dimensions of the channels and the number of free-standing walls can easily be varied by varying the different etching times and the number of times the potential is switched. We encountered considerable problems concerning the mechanical stability of the membrane in the "conventional" structures. The "buried layer" is more stable because the porous layer is attached to an immovable structure. The pore size of the PS was approximately 7 nm, as estimated from FEGSEM pictures.

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